

# INV100FQ030C

100V Bi-directional Enhancement-mode GaN Power Transistor

## INV100FQ030C

### 1. General description

Bi-directional GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in FCQFN with 4.0 mm x 6.0 mm package size.

### 2. Features

- Bi-directional blocking capability
- GaN-on-Silicon E-mode HEMT technology
- Ultra-low on resistance

### 3. Applications

- BMS battery protection
- High side load switch in bi-directional converter
- Switch circuits in multiple power supplier system

### 4. Key performance parameters

Table 1 Key performance parameters at  $T_J = 25\text{ }^\circ\text{C}$

Parameter	Value	Unit
$V_{DD, \max}$	100	V
$R_{DD(\text{on}), \max} @ V_G = 5\text{ V}$	3.2	m $\Omega$
$Q_{G, \text{typ}} @ V_{DD} = 50\text{ V}$	66	nC
$I_{D, DC} (T_A=25\text{ }^\circ\text{C})$	100	A

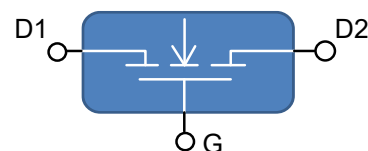
### 5. Pin information

Table 2 Pin information

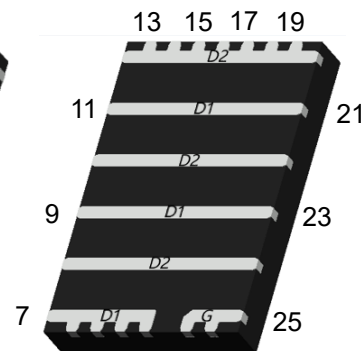
Pin	Pin description	Pin function
1,2,25	Gate	Driver Gate
3-7,9,11,21,23	Drain1	Power Drain1
8,10,12-20,22,24	Drain2	Power Drain2

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INV100FQ030C	FCQFN 4X6	J30



Top View



Bottom View

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## 6. Maximum ratings

at  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscence sales office.

**Table 4** Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
$V_{DD}$	Drain1-to-Drain2 Voltage or Drain2-to-Drain1 Voltage	100	V
$V_{DD(tr)}$	Drain1-to-Drain2 Voltage or Drain2-to-Drain1 Voltage <sup>1</sup> ( $V_G=0V$ , 1h total time, $T_A=T_{JMAX}$ )	120	V
$V_{DG}$	Drain1-to-Gate Voltage or Drain2-to-Gate Voltage	100	V
$V_{GD}$	Gate-to-Drain1 Voltage or Gate-to-Drain2 Voltage	6	V
$I_D$	Continuous Drain Current ( $T_A=25^\circ\text{C}$ )	100	A
$I_{DM}$	Pulsed Drain Current ( $T_A=25^\circ\text{C}$ , $T_{Pulse} = 100\ \mu\text{s}$ )	320	A
$T_J$	Operating Temperature	-40 to 150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	-40 to 150	$^\circ\text{C}$

Note:

1. Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation;

### 7. Thermal characteristics

**Table 5 Thermal characteristics**

SYMBOL	PARAMETER	TYP	UNIT	Note/Test Condition
$R_{\theta JC}$	Thermal Resistance, Junction to Case	12.09	°C/W	
$R_{\theta JB}$	Thermal Resistance, Junction to Board	1.64	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient <sup>2</sup>	61.34	°C/W	
$T_{sold}$	Maximum reflow soldering temperature	260	°C	MSL3

Note:

- $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

## 8. Electric characteristics

at  $T_J = 25\text{ }^\circ\text{C}$ , unless specified otherwise

**Table 6** Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
$I_{D1D2}$	Drain1-to-Drain2 Leakage	-	1	4	$\mu\text{A}$	$V_{D2} = V_G = 0\text{ V}$ , $V_{D1} = 80\text{ V}$
$I_{D2D1}$	Drain2-to-Drain1 Leakage	-	1	4	$\mu\text{A}$	$V_{D1} = V_G = 0\text{ V}$ , $V_{D2} = 80\text{ V}$
$I_{GD}$	Gate-to-Drain Forward Leakage	-	1	4	$\mu\text{A}$	$V_{D1} = V_{D2} = 0\text{ V}$ , $V_G = 5\text{ V}$
	Gate-to-Drain Forward Leakage		2	8	$\mu\text{A}$	$V_{D1} = V_{D2} = 0\text{ V}$ , $V_G = 5.5\text{ V}$
	Gate-to-Drain Forward Leakage	-	4.5	18	$\mu\text{A}$	$V_{D1} = V_{D2} = 0\text{ V}$ , $V_G = 6\text{ V}$
$V_{GD1(TH)}$	Gate Threshold Voltage	0.8	1.1	2.5	V	$V_{D1} = 0\text{ V}$ , $V_{D2} = V_G$ , $I_{D2D1} = 11.5\text{ mA}$
$V_{GD2(TH)}$	Gate Threshold Voltage	0.8	1.1	2.5	V	$V_{D2} = 0\text{ V}$ , $V_{D1} = V_G$ , $I_{D1D2} = 11.5\text{ mA}$
$R_{D1D2(on)}$	Drain1-to-Drain2 On-state Resistance <sup>3</sup>	-	2.5	3.2	$\text{m}\Omega$	$V_{D2} = 0\text{ V}$ , $V_{GD} = 5\text{ V}$ , $I_{D1D2} = 25\text{ A}$
$R_{D2D1(on)}$	Drain2-to-Drain1 On-state Resistance <sup>3</sup>	-	2.5	3.2	$\text{m}\Omega$	$V_{D1} = 0\text{ V}$ , $V_{GD} = 5\text{ V}$ , $I_{D2D1} = 25\text{ A}$

Note:

- $R_{DS(on)}$  is measured without prior drain bias or switching stress.

**Table 7 Dynamic characteristics <sup>4</sup>**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C <sub>ISS</sub>	Input Capacitance	-	2770	-	pF	V <sub>G</sub> = 0 V, V <sub>D</sub> = 50 V
C <sub>OSS</sub>	Output Capacitance	-	620	-		
C <sub>RSS</sub>	Reverse Transfer Capacitance	-	310	-		
R <sub>G</sub>	Gate Resistance	-	5.2	-	Ω	f = 5 MHz, Open drain
Q <sub>G</sub>	Total Gate Charge	-	66	-	nC	V <sub>D</sub> = 50 V, V <sub>G</sub> = 5 V, I <sub>D</sub> = 25 A
Q <sub>GD1</sub>	Gate-to-Drain1 Charge (V <sub>D2D1</sub> =50V)	-	4.4	-		V <sub>D1</sub> = 0, V <sub>D2</sub> = 50 V, I <sub>D2D1</sub> = 25 A
Q <sub>GD1</sub>	Gate-to-Drain1 Charge (V <sub>D1D2</sub> =50V)	-	44	-		V <sub>D2</sub> = 0, V <sub>D1</sub> = 50 V, I <sub>D1D2</sub> = 25 A
Q <sub>GD2</sub>	Gate-to-Drain2 Charge (V <sub>D1D2</sub> =50V)	-	4.4	-		V <sub>D2</sub> = 0, V <sub>D1</sub> = 50 V, I <sub>D1D2</sub> = 25 A
Q <sub>GD2</sub>	Gate-to-Drain2 Charge (V <sub>D2D1</sub> =50V)	-	44	-		V <sub>D1</sub> = 0, V <sub>D2</sub> = 50 V, I <sub>D2D1</sub> = 25 A
Q <sub>OSS</sub>	Output Charge	-	62	-		V <sub>G</sub> = 0 V, V <sub>D</sub> = 50 V
Q <sub>rr</sub>	Reverse recovery charge	-	0	-		V <sub>D</sub> = 50 V, I <sub>D</sub> = 25 A

Note:

4. Guaranteed by design.

## 9. Electric characteristics diagrams

at  $T_J = 25^\circ\text{C}$  unless otherwise specified.

Note: In Charts,  $V_{D1D2}$  can be  $V_{D2D1}$  with same characteristic chart due to Bi-directional feature.

Fig. 1 Typical Output Characteristics ( $T_J=25^\circ\text{C}$ )

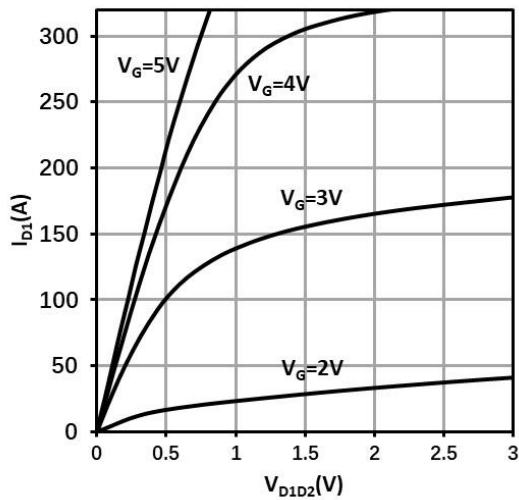


Fig. 2 Typical Output Characteristics ( $T_J=125^\circ\text{C}$ )

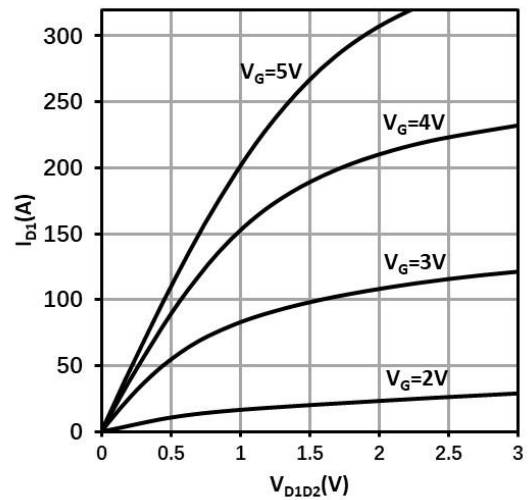


Fig.3 Typical Drain On-state Resistance ( $T_J=25^\circ\text{C}$ )

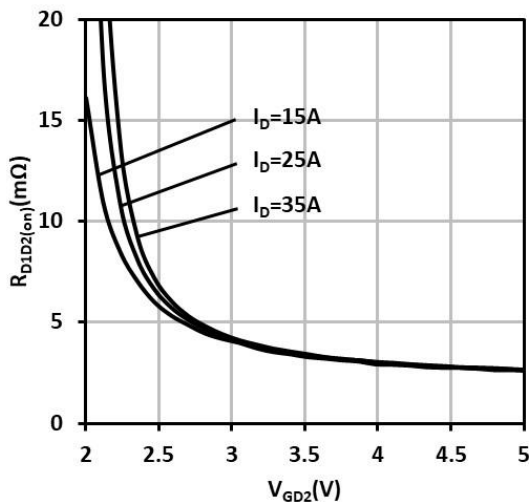


Fig. 4 Typical Drain On-state Resistance ( $T_J=125^\circ\text{C}$ )

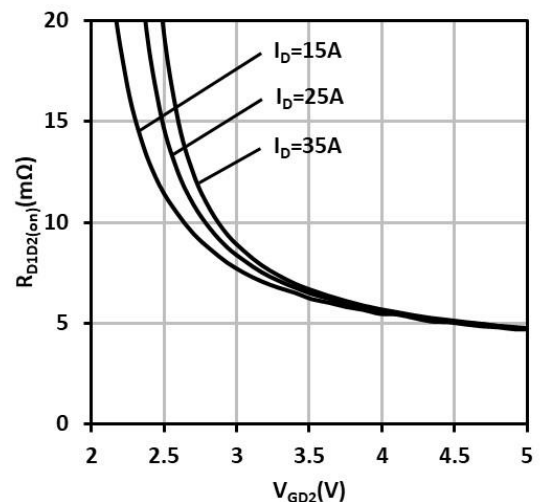


Fig. 5 Normalized On-State Resistance vs. Temp.

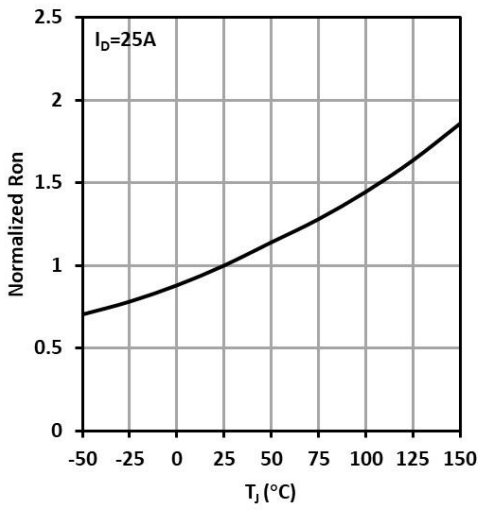


Fig. 6 Typical Transfer Characteristics

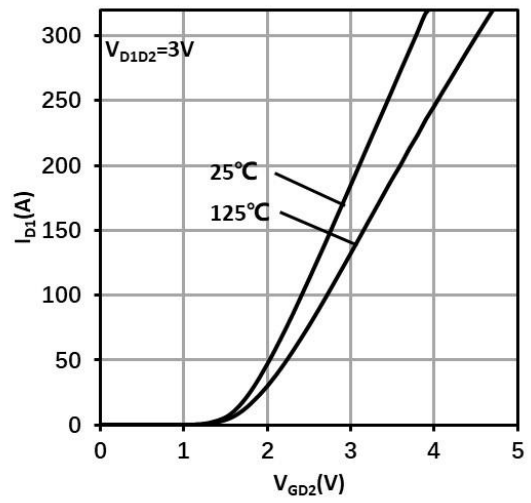


Fig. 7 Typ. Reverse Drain1-Drain2 Characteristics ( $V_{GD2} \leq 0, T_J = 25^\circ C$ )

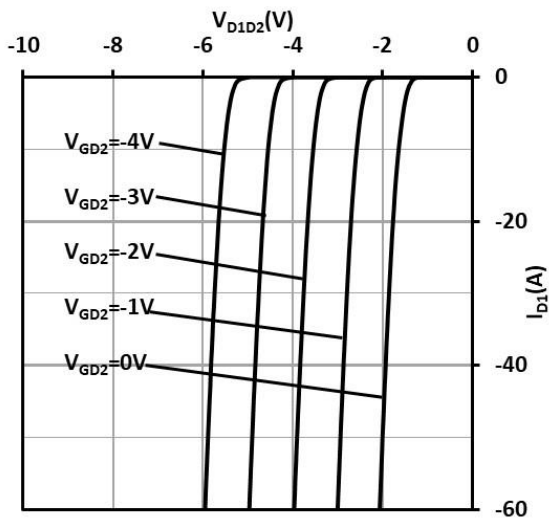
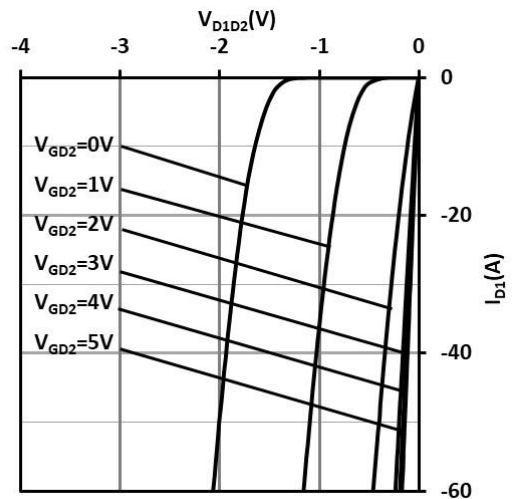


Fig. 8 Typ. Reverse Drain1-Drain2 Characteristics ( $V_{GD2} \geq 0, T_J = 25^\circ C$ )





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Fig. 9 Typ. Reverse Drain1-Drain2 Characteristics ( $V_{GD2} \leq 0$ ,  $T_J = 125^\circ\text{C}$ )

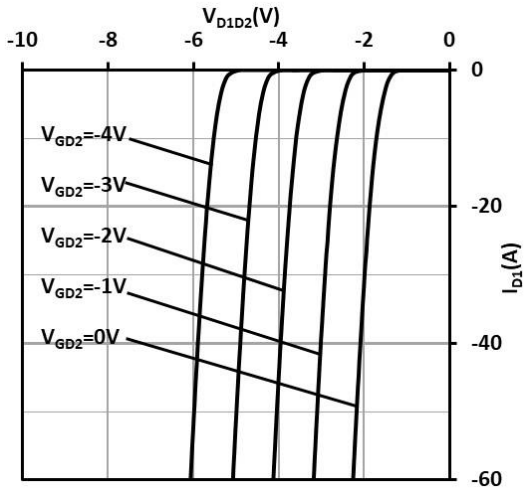


Fig. 10 Typ. Reverse Drain1-Drain2 Characteristics ( $V_{GD2} \geq 0$ ,  $T_J = 125^\circ\text{C}$ )

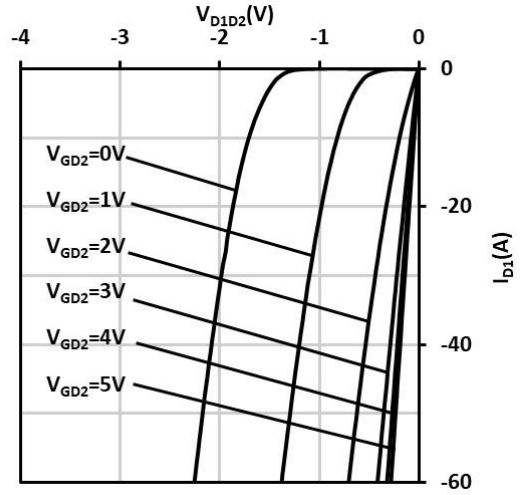


Fig. 11 Typ. Capacitances Characteristics

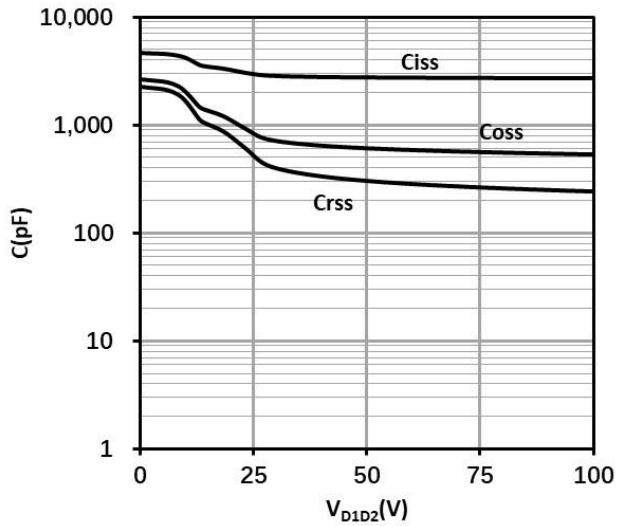


Fig. 12 Typ. Gate Charge

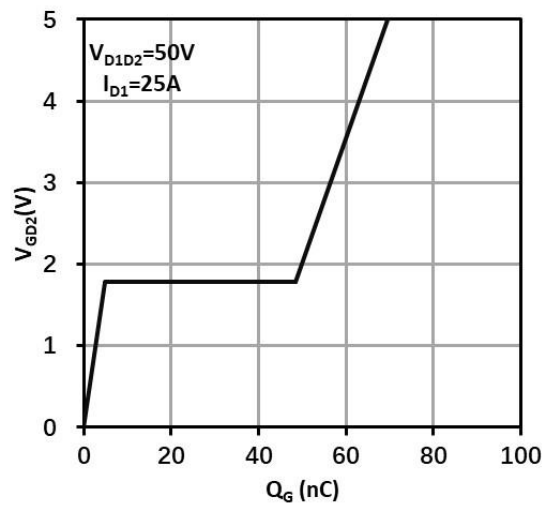


Fig. 13 Normalized Threshold Voltage vs. Temp.

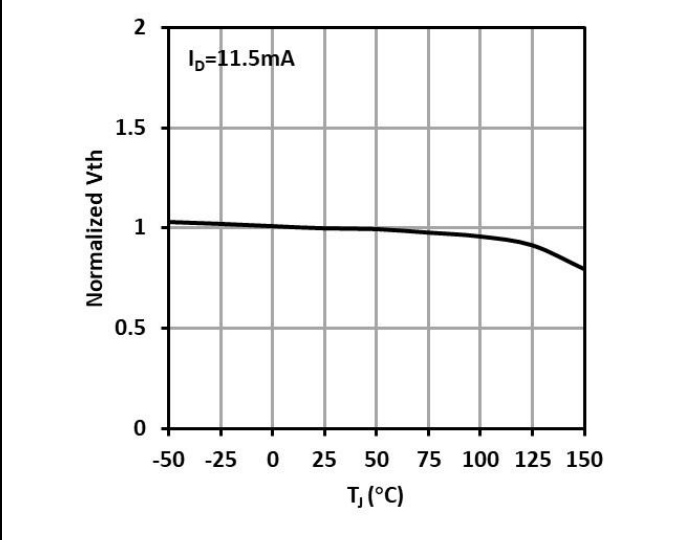


Fig. 14 Output Charge

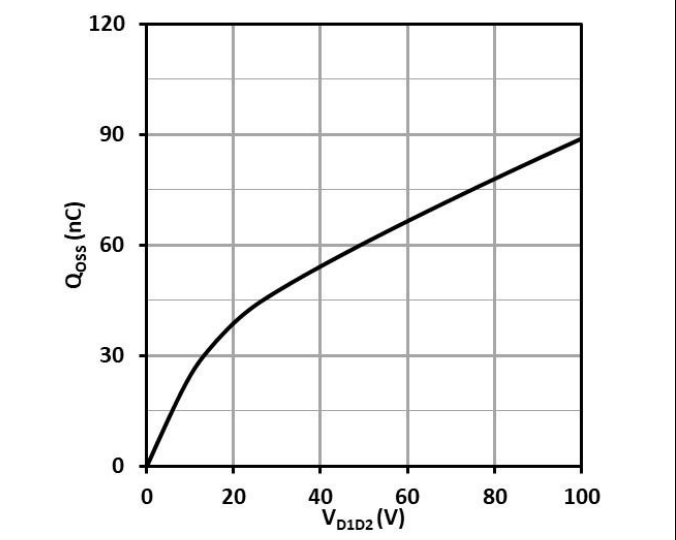


Fig. 15 Output Capacitance Stored Energy

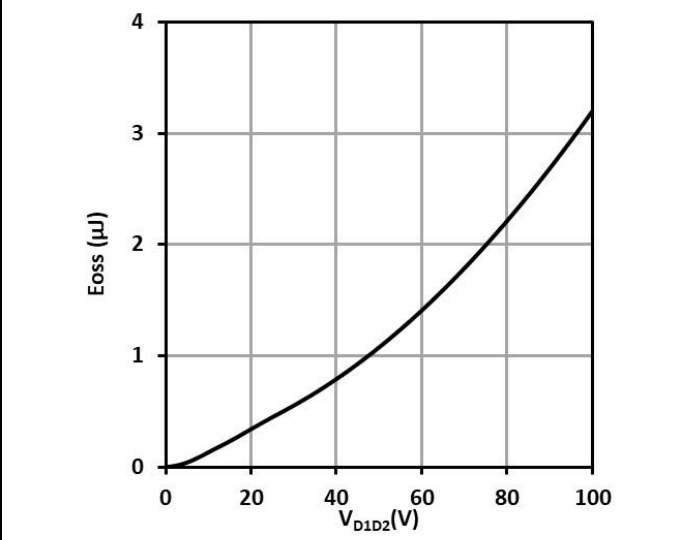


Fig. 16 Power Dissipation

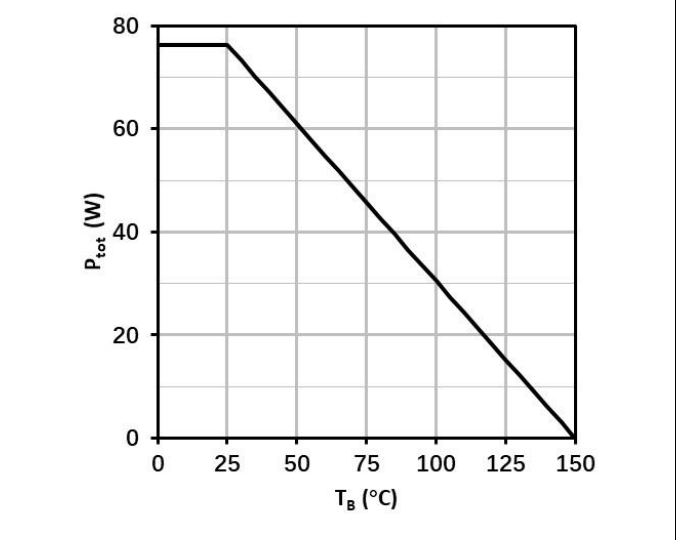


Fig. 17 Safe Operating Area

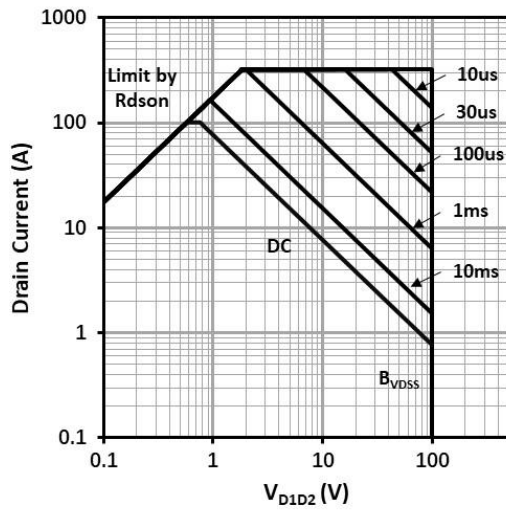
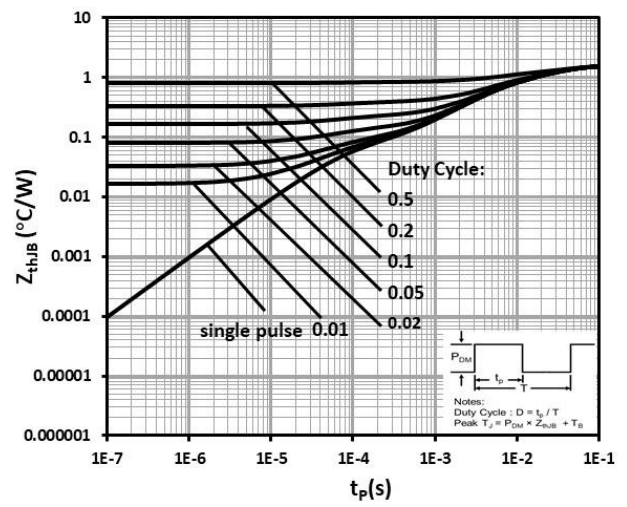
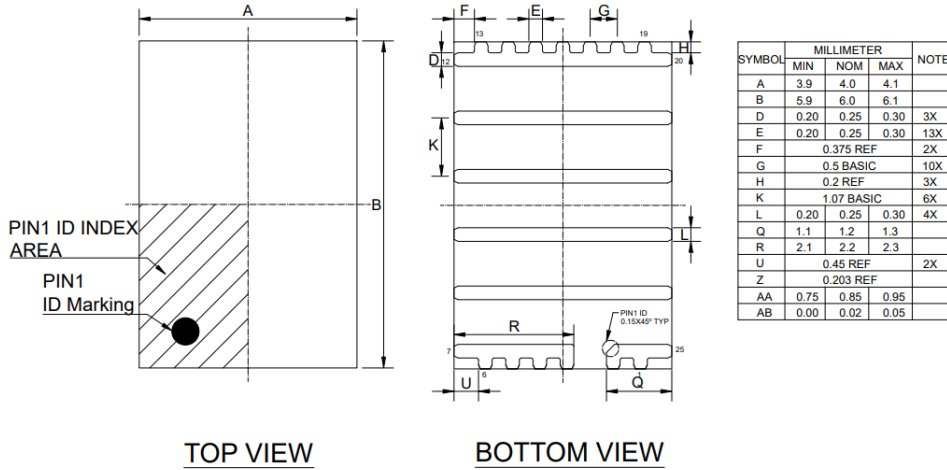


Fig. 18 Max. Transient Thermal Impedance



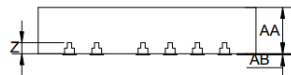
### 10. Package outlines

#### Package Reference



TOP VIEW

BOTTOM VIEW

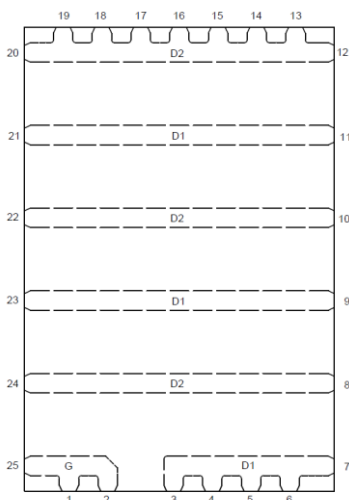


SIDE VIEW

#### NOTE:

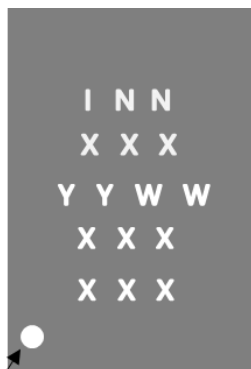
- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 3) JEDEC REFERENCE IS MO-220.
- 4) DRAWING IS NOT TO SCALE.

#### PIN configuration



TOP VIEW

#### Marking Reference



Die Orientation Dot  
& Gate Position

Row	Description	Example
Row 1	Company name	INN
Row 2	Product code	XXX
Row 3	Date code	YYWW
Row 4	Lot No	XXX
Row 5	Lot No	XXX

### 11. Reel information

NOTES:

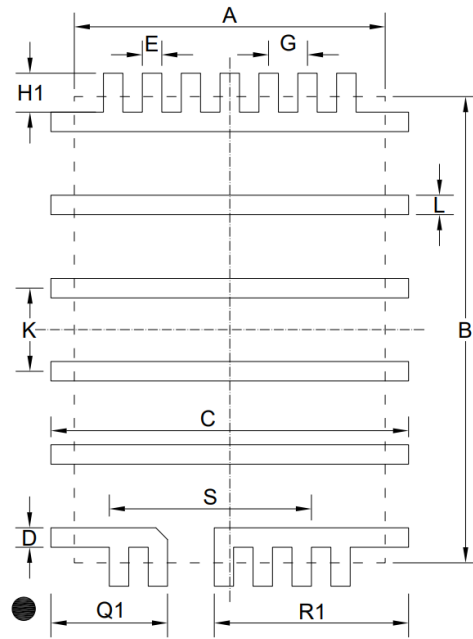
1. CARRIER TAPE COLOR: BLACK.
2. COVER TAPE WIDTH: 13.3±0.10.
3. COVER TAPE COLOR: TRANSPARENT.
4. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20 MAX.
5. CAMBER NOT TO EXCEED 1MM IN 100MM.
6. MOLD# QFN/DFN/MIS6X4X0.75/0.85.
7. ALL DIMS IN MM.
8. BAN TO USE THE ENVIRONMENT-RELATED SUBSANCES OF JCET PRESCRIBING.

NOTES:

1. 2500 UNITS PER TRAY.
2. COLOR: WHITE.
3. ALL DIM IN mm.
4. GENERAL TOLERANCE±0.25.
5. BAN TO USE THE ENVIRONMENT-RELATED SUBSANCES OF JCET PRESCRIBING.
6. THE DERECTION OF VIEW:

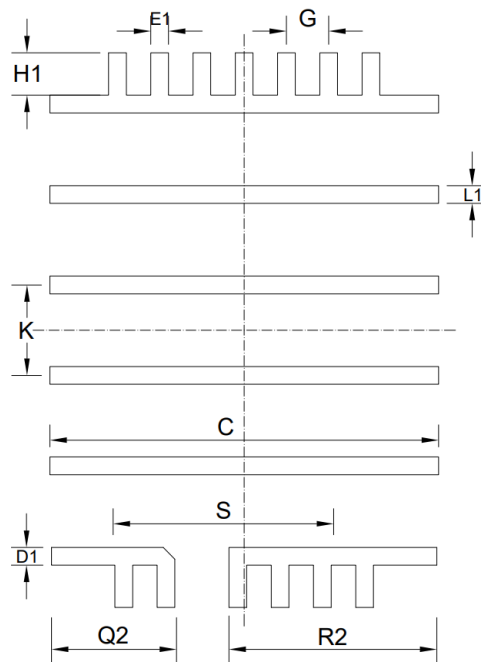
## 12. Land pattern

### Recommended Land Pattern



SYMBOL	MILLIMETER	NOTE
A	4.0	
B	6.0	
C	4.6	5X
D	0.25	3X
E	0.25	13X
G	0.5	10X
H1	0.5	13X
K	1.07	6X
L	0.25	4X
R1	2.5	
Q1	1.5	
S	2.6	

### Recommended Stencil drawing



SYMBOL	MILLIMETER	NOTE
C	4.56	5X
D1	0.21	3X
E1	0.21	13X
G	0.5	10X
H1	0.5	13X
K	1.07	6X
L1	0.21	4X
R2	2.46	
Q2	1.46	
S	2.6	

### 13. Revision history

**Major changes since the last revision**

Revision	Date	Description of changes
1.0	2024-08-05	1.0 version release

## Important Notice

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